

AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 1, 6, 13, 16, 18-21, 24, 26, 29, 32, 33 and 42, as shown below.

The following is a complete list of all claims in this application.

1. (Currently Amended) A method for manufacturing a ~~wire~~ contact structure, comprising steps of:

forming a ~~wire-made~~ first conductive layer formed of an aluminum-based material;

depositing a silicon nitride layer ~~on the wire~~ at a temperature between about 280° C and about 400° C ~~to form an insulating layer~~;

forming a contact hole extending through the ~~insulating~~ silicon nitride layer and exposing the ~~wire~~ first conductive layer; and

forming a second conductive layer formed of indium zinc oxide (IZO) and directly contacting the ~~wire~~ first conductive layer through the contact hole.

2-3. (Cancelled)

4. (Previously Presented) The method of claim 1, wherein the step of depositing the silicon nitride layer is performed for about 5 minutes to about 40 minutes.

5. (Previously Presented) The method of claim 1, wherein the contact hole has a size between about 0.5 mm X 15 μm and 2 mm X 60 μm .

6. (Currently Amended) The method of claim 1, wherein a contact resistance between the ~~aluminum-based material~~ first conductive layer and the ~~IZO~~ second conductive layer is less than 10% of a ~~wire~~ resistance of the ~~wire~~ first conductive layer.

7. (Original) The method of claim 6, wherein the contact resistance is less than 0.15 $\mu\Omega\text{cm}^2$.

8–12. (Cancelled)

13. (Currently Amended) A method for manufacturing a thin film transistor (TFT) array panel, comprising steps of:

depositing a first conductive layer formed of ~~forming a gate wire formed of an~~
~~aluminum-based material on a substrate, the gate wire including a gate pad;~~

patterning the first conductive layer to form a gate line and a gate pad connected to the gate line;

depositing a silicon nitride layer over the gate wire on the gate line and a gate pad at a temperature between about 280° C and about 400° C ~~to form a gate-insulating layer;~~

forming a semiconductor layer on the gate-insulating silicon nitride layer;

depositing a second conductive layer ~~forming a data wire~~ on the semiconductor layer;

patterning the second conductive layer to form a data line;

forming a contact hole extending through the ~~gate-insulating~~ silicon nitride layer and exposing the gate pad;

depositing a third conductive layer formed of an indium zinc oxide (IZO) layer ~~on the gate pad and the data wire~~; and

patterning the ~~IZO~~ third conductive layer to form a conductive layer pattern directly contacting the gate pad in the contact hole.

14-15. (Cancelled)

16. (Currently Amended) The method of claim 13, wherein the step of depositing the ~~IZO~~ third conductive layer comprises a step of sputtering a compound including In_2O_3 and ZnO .

17. (Previously Presented) The method of claim 16, wherein a content rate of Zn in the compound is between about 15% and about 20%.

18. (Currently Amended) The method of claim 13, wherein the step of patterning the ~~IZO~~ third conductive layer comprises a step of forming a pixel electrode connected to the data wire line.

19. (Currently Amended) A method for manufacturing a thin film transistor array panel, comprising steps of:

depositing a first conductive layer formed of an aluminum-based material on a substrate;

patterning the first conductive layer to form ~~forming a gate wire formed of an aluminum-based material on a substrate, the gate wire comprising a gate line, a gate electrode and a gate pad;~~

depositing a silicon nitride layer at a temperature between about 280° C and about 400° C ~~to form a gate insulating layer;~~

forming a semiconductor layer on the ~~gate insulating~~ silicon nitride layer;

depositing a second conductive layer over the silicon nitride layer and the semiconductor layer;

patterning the second conductive layer to form ~~forming a data wire including a data line, a source electrode and a drain electrode;~~

forming a passivation layer over the ~~gate insulating~~ silicon nitride layer and the data wire;

forming a contact hole extending through the passivation layer and the ~~ate insulating~~ silicon nitride layer and exposing the gate pad;

depositing a third conductive layer formed of an indium zinc oxide (IZO) layer over the passivation layer; and

patterning the IZO third conductive layer to form a redundant gate pad directly contacting the gate pad through the contact hole.

20. (Currently Amended) The method of claim 19, wherein the step of patterning the IZO third conductive layer comprises a step of ~~forming~~ patterning the third conductive layer to form a pixel electrode.

21. (Currently Amended) The method of claim 19, wherein the ~~data wire~~ further comprises step of patterning the second conductive layer comprises a step of patterning the second conductive layer to form a data pad, and

the step of patterning the IZO third conductive layer comprises a step of ~~forming~~ patterning the third conductive layer to form a redundant data pad connected to the data pad.

22. (Previously Presented) The method of claim 19, wherein the step of forming the passivation layer comprises a step of depositing a silicon nitride layer at a temperature between about 280° C and about 400° C.

23. (Cancelled)

24. (Currently Amended) The method of claim 19, wherein the step of depositing the IZO third conductive layer comprises a step of sputtering a compound including In_2O_3 and ZnO .

25. (Previously Presented) The method of claim 24, wherein a content rate of Zn in the compound is between about 15% and about 20%.

26. (Currently Amended) The method of claim 19, wherein the step of patterning the second conductive layer comprises a step of patterning the semiconductor layer and the second conductive layer simultaneously by using data-wire and the semiconductor layer are simultaneously patterned by a photoresist pattern having portions with different thicknesses.

27. (Previously Presented) The method of claim 26, wherein the photoresist pattern comprises a first portion having a first thickness, a second portion having a second thickness greater than the first thickness, and a third portion having a third thickness smaller than the first thickness.

28. (Previously Presented) The method of claim 27, wherein a mask used for forming the photoresist pattern has a first area having a first transmittance, a second area having a second transmittance smaller than the first transmittance, and a third area having a third transmittance greater than the first transmittance.

29. (Currently Amended) The method of claim 28, wherein the first portion of the photo resist pattern is aligned on a portion between the source electrode and the drain electrode, and the second portion of the photoresist pattern is aligned on the data line wire.

30. (Previously Presented) The method of claim 29, wherein the first area of the mask includes a partially transparent layer or a pattern reducing a transmittance.

31. (Previously Presented) The method of claim 30, wherein the first thickness is less than a half of the second thickness.

32. (Currently Amended) The method of claim 31, further comprising a step of depositing an ohmic contact layer between the ~~data-wire~~ source and drain electrodes and the semiconductor layer.

33. (Currently Amended) The method of claim 32, wherein the ~~data-wire~~ second conductive layer, the ohmic contact layer, and the semiconductor layer are patterned by a single photolithography process.

34 – 41. (Cancelled)

42. (Currently Amended) A method for manufacturing a contact structure, comprising steps of:

depositing ~~forming~~ a ~~wire~~ first conductive layer formed of aluminum on a substrate;

patterning the first conductive layer to form a signal line;

depositing a silicon nitride layer on the ~~wire~~ signal line at a fixed temperature between about 280° C and about 400° C;

forming a contact hole extending through the silicon nitride layer and exposing the wire signal line; and

forming a second conductive layer formed of indium zinc oxide (IZO) and ~~electrically connected to~~ directly contacting the wire signal line through the contact hole.